

**10 Pulse 1/4 wafer**

Trench Width (um)	Actual Width (um)	Etch Depth (um)	Etch Rate (um/pulse)	Undercut Etch (um)	Undercut Rate (um/pulse)	Undercut:Depth Ratio
1	1.98	4.56	0.456	3.88	0.388	0.8509
2	2.45	4.61	0.461	3.98	0.398	0.8633
5	5.41	5.21	0.521	4.37	0.437	0.8388
10	10.16	5.85	0.585	4.95	0.495	0.8462
25	24.78	6.78	0.678	5.24	0.524	0.7729
250		10.5	1.05			
1000		5	0.5			

**25 Pulse 1/4 wafer**

Trench Width (um)	Actual Width (um)	Etch Depth (um)	Etch Rate (um/pulse)	Undercut Etch (um)	Undercut Rate (um/pulse)	Undercut:Depth Ratio
1	1.8	8.42	0.3368	6.48	0.2592	0.7696
2	2.74	8.99	0.3596	7.07	0.2828	0.7864
5	5.59	10.53	0.4212	7.95	0.318	0.7550
10	10.39	12.76	0.5104	9.98	0.3992	0.7821
25	25.15	17.58	0.7032	13.85	0.554	0.7878
250		25.5	1.02			
1000		13	0.52			

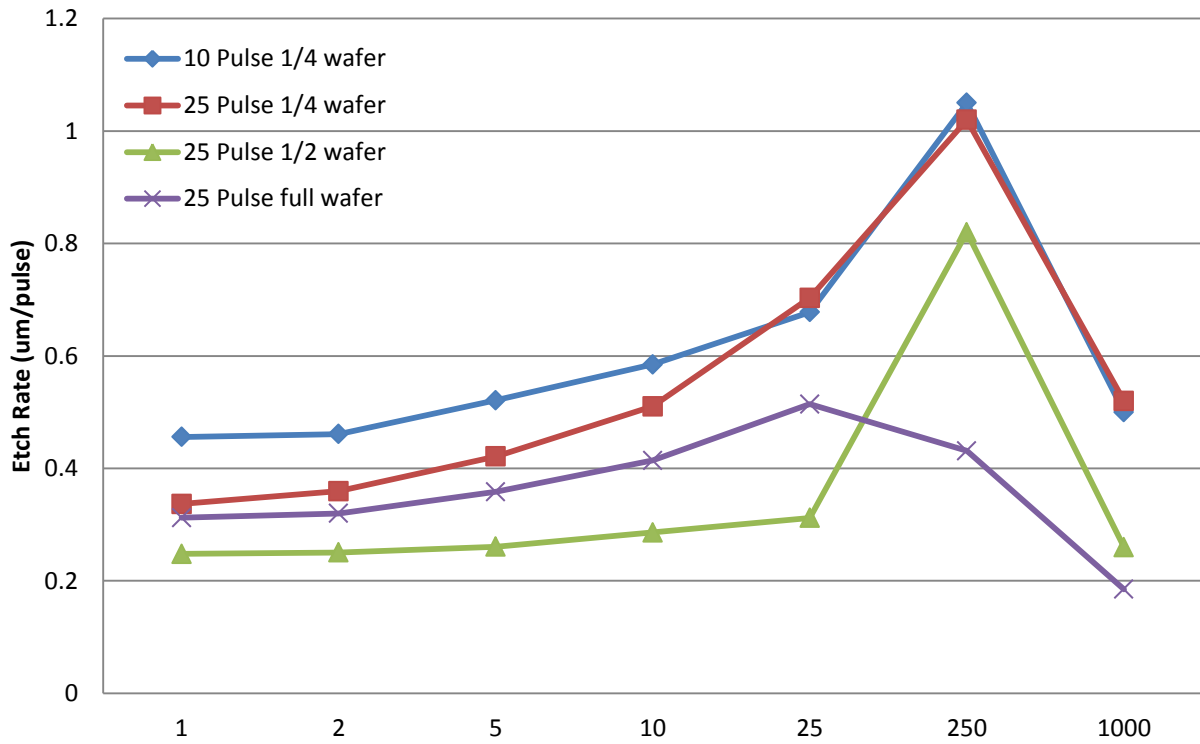
**25 Pulse 1/2 wafer**

Trench Width (um)	Actual Width (um)	Etch Depth (um)	Etch Rate (um/pulse)	Undercut Etch (um)	Undercut Rate (um/pulse)	Undercut:Depth Ratio
1	2.13	6.2	0.248	5.4	0.216	0.8710
2	2.51	6.26	0.2504	5.5	0.22	0.8786
5	5.59	6.52	0.2608	5.88	0.2352	0.9018
10	10.35	7.15	0.286	6.53	0.2612	0.9133
25	24.45	7.8	0.312	7.68	0.3072	0.9846
250		20.5	0.82			
1000		6.5	0.26			

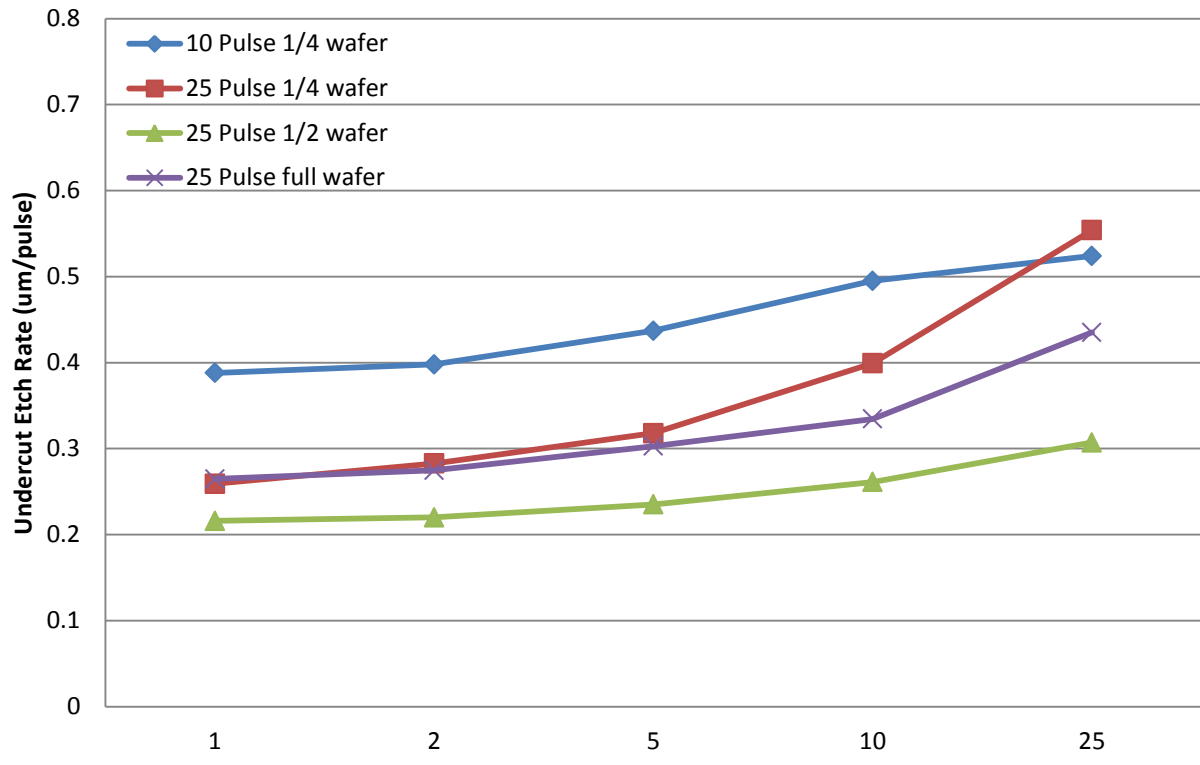
**25 Pulse full wafer**

Trench Width (um)	Actual Width (um)	Etch Depth (um)	Etch Rate (um/pulse)	Undercut Etch (um)	Undercut Rate (um/pulse)	Undercut:Depth Ratio
1	1.72	7.81	0.3124	6.62	0.2648	0.8476
2	2.65	8	0.32	6.87	0.2748	0.8588
5	5.47	8.96	0.3584	7.57	0.3028	0.8449
10	10.1	10.35	0.414	8.36	0.3344	0.8077
25	24.74	12.86	0.5144	10.88	0.4352	0.8460
250		10.78	0.4312			
1000		4.63	0.1852			

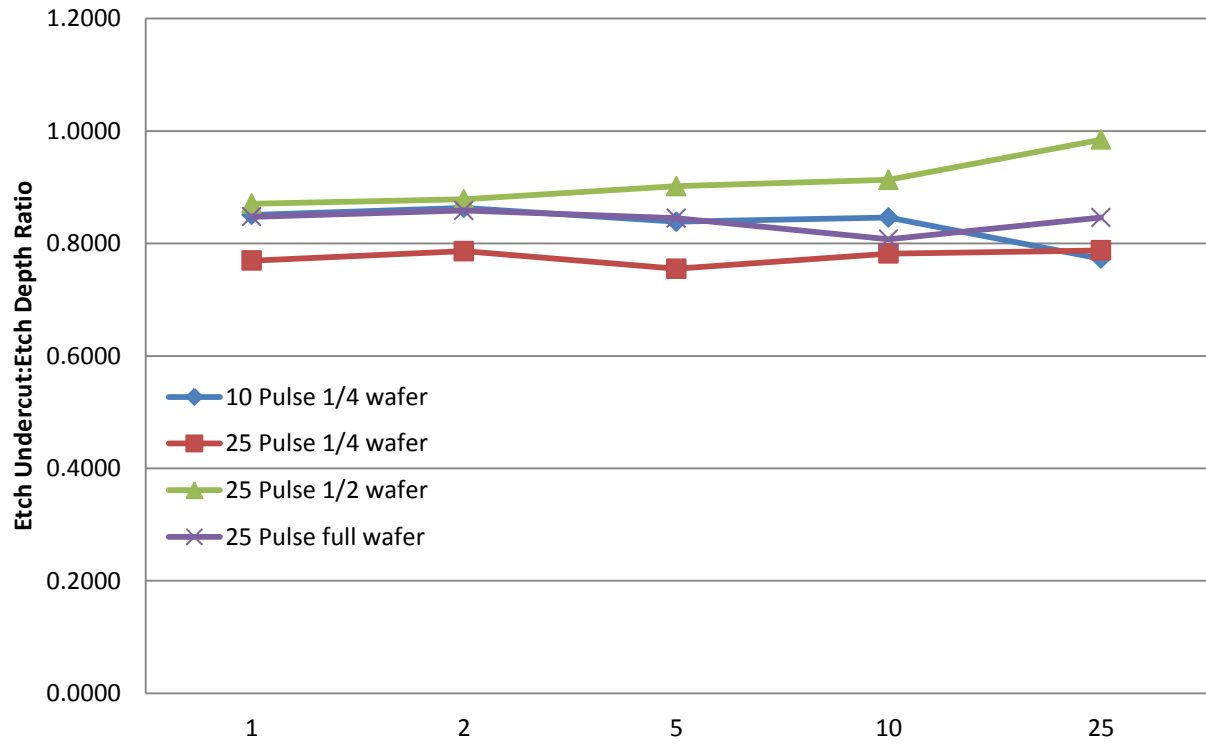
### Etch Rates vs Trench Width

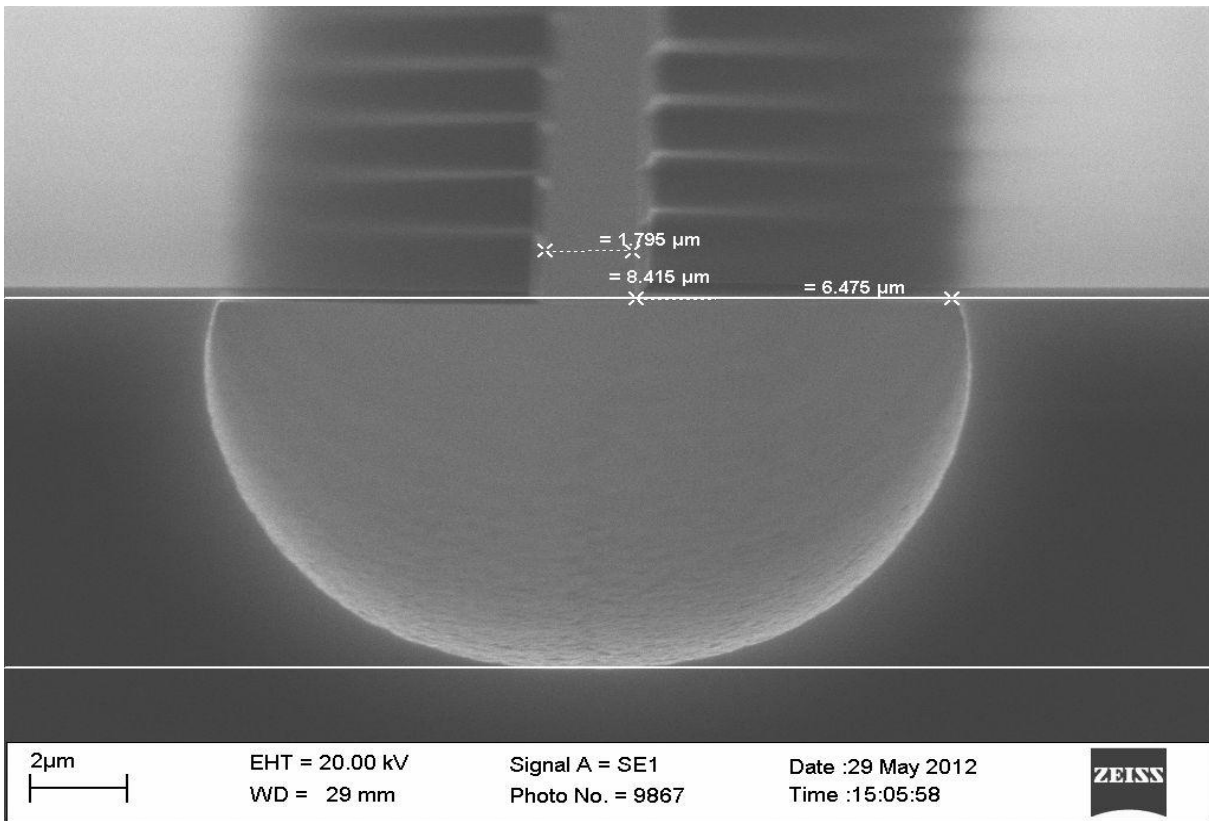


### Undercut Rates vs Trench Width

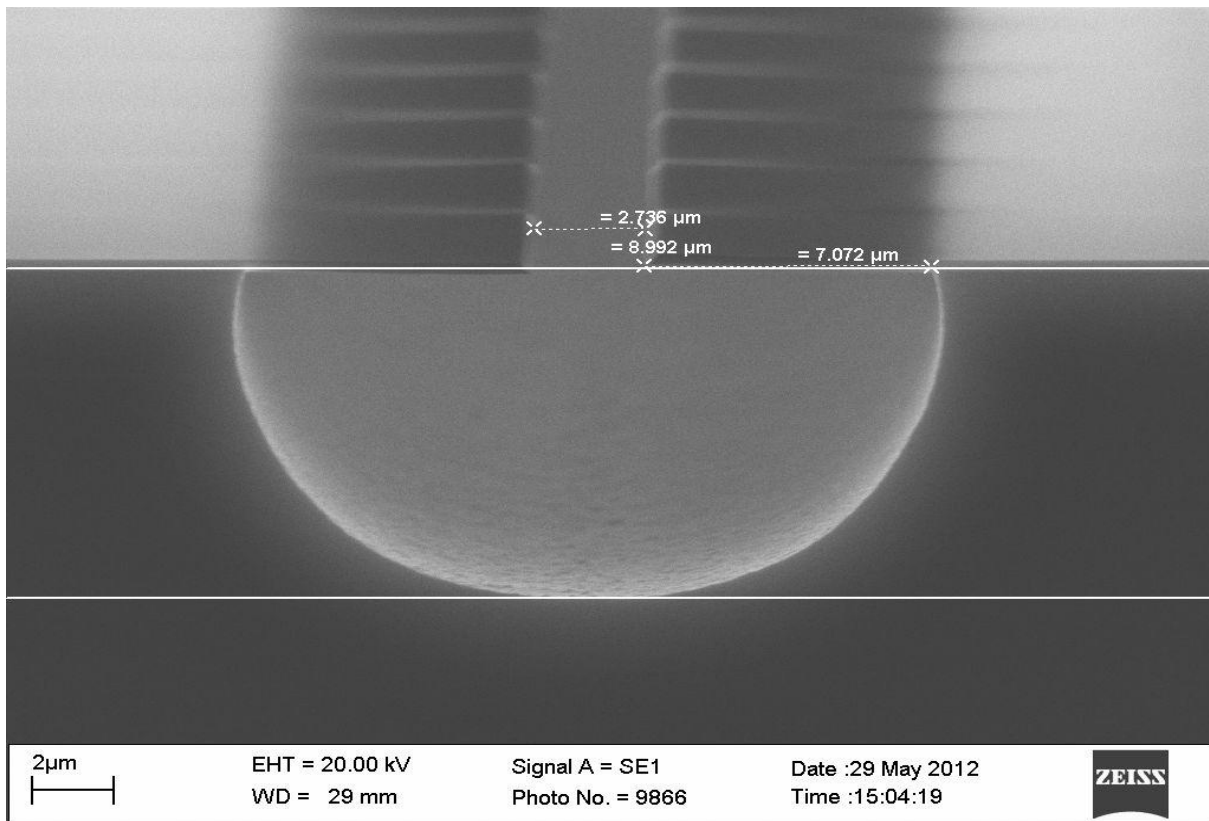


# Undercut vs Depth Ratio

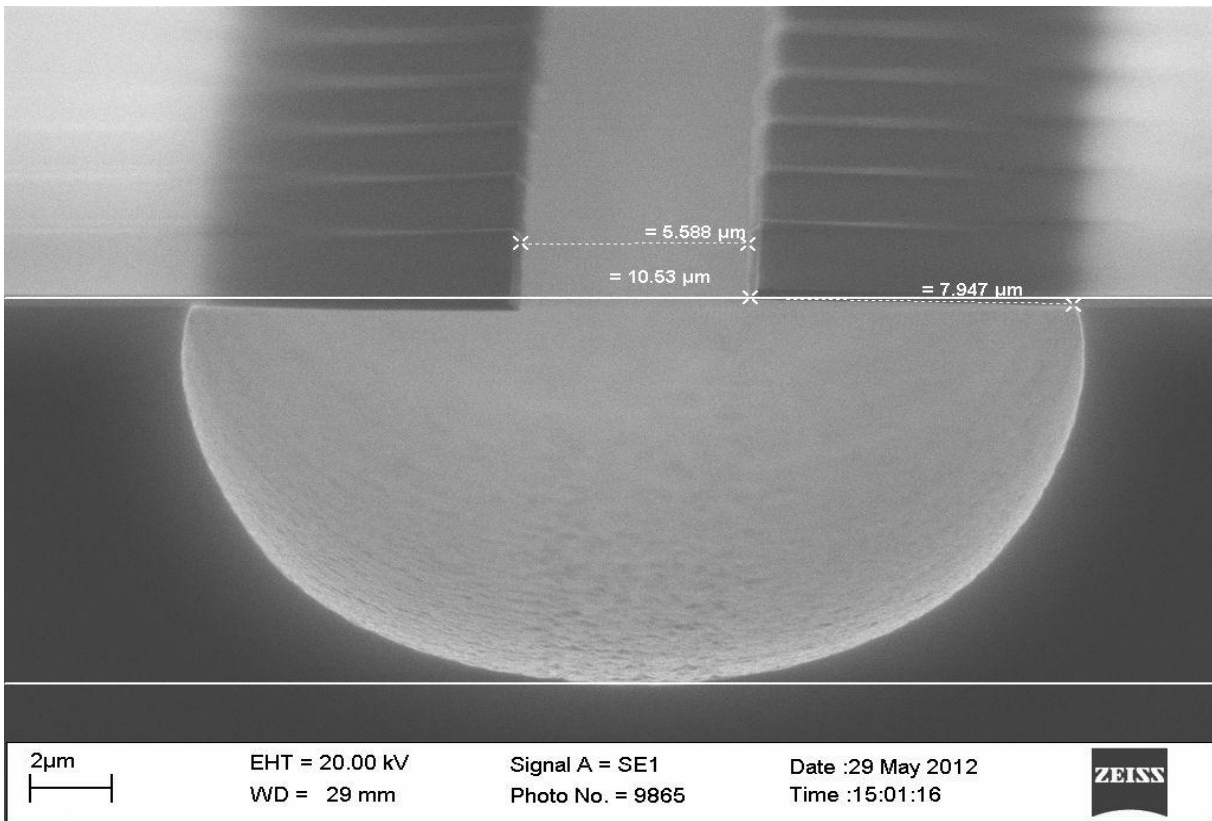




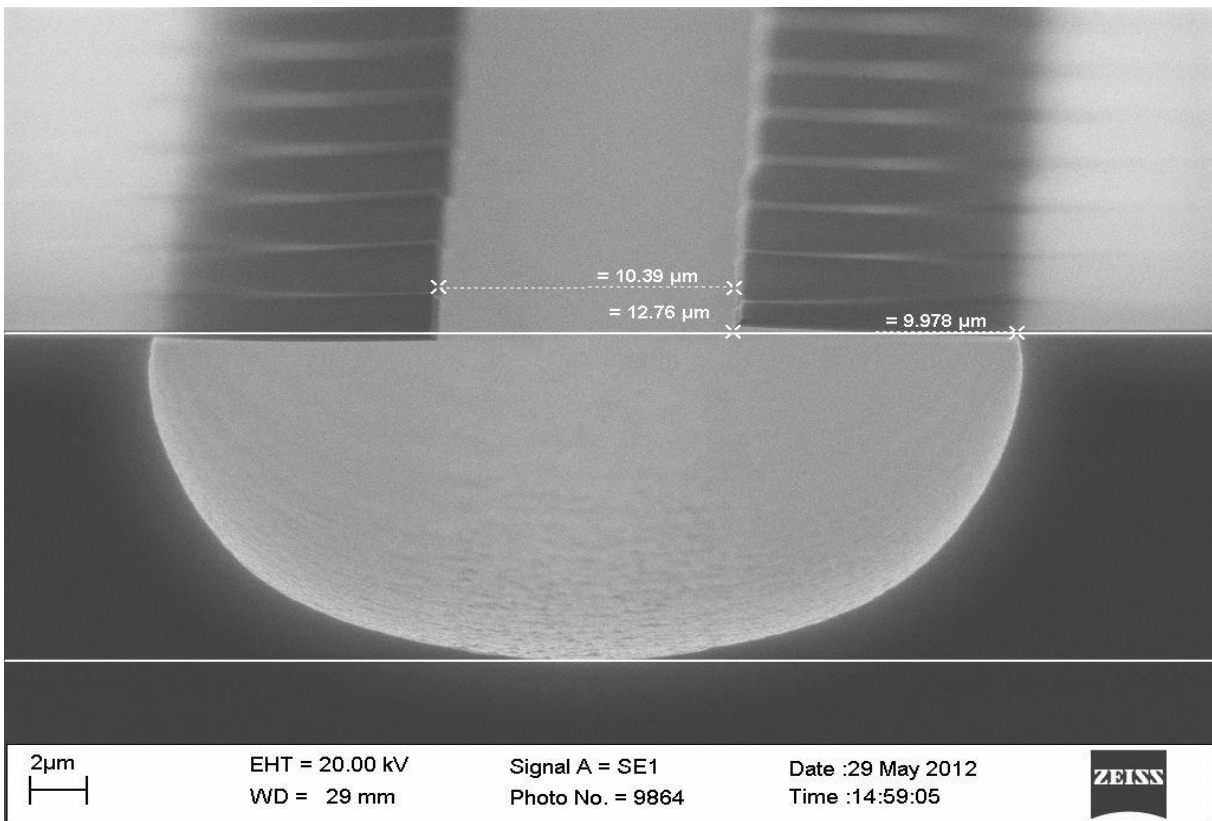
Quarter wafer, 25 pulse, 1µm trench



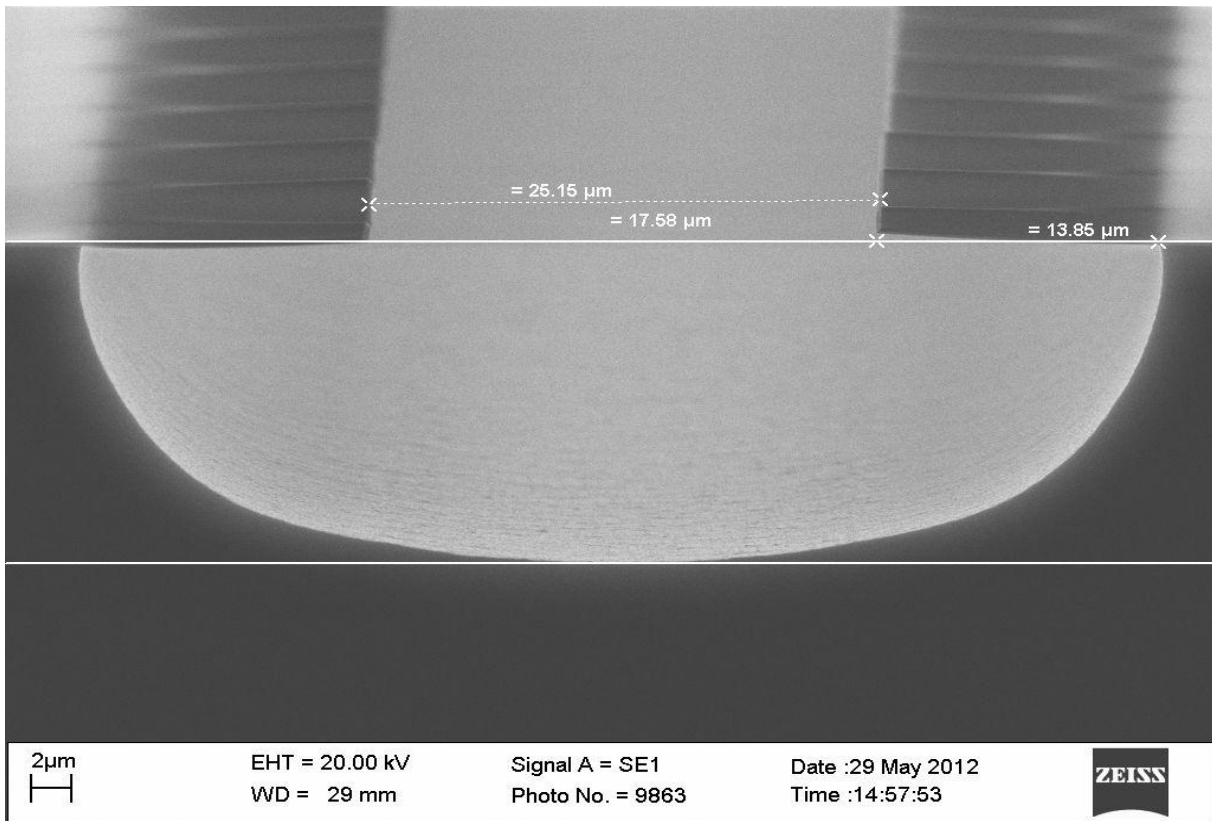
Quarter wafer, 25 pulse, 2µm trench



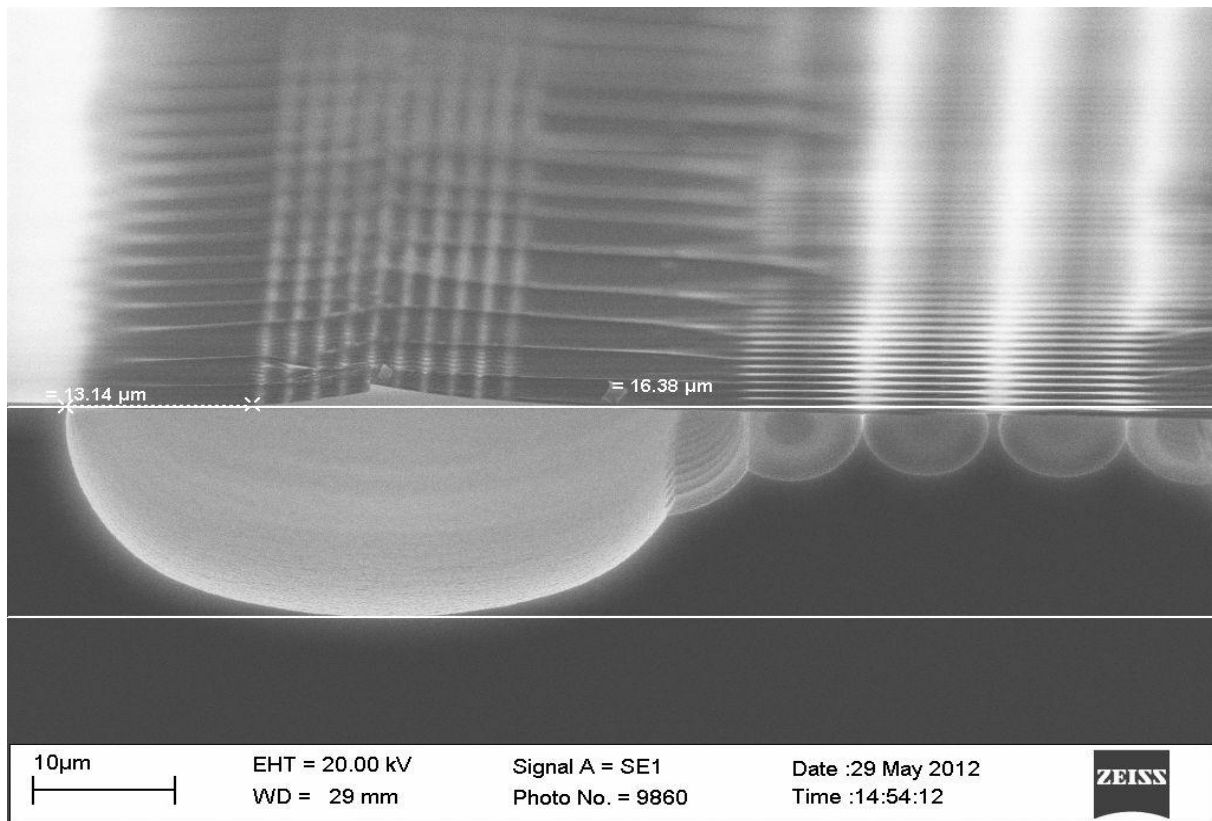
Quarter wafer, 25 pulse, 5um trench



Quarter wafer, 25 pulse, 10um trench



Quarter wafer, 25 pulse, 25um trench



Quarter Wafer, 25 pulse, 1um vias low mag. Left features are 1um vias with 1um spacing, in a series of 10.

**Notes**

Wafer prep - Two thermally oxidized wafers were patterned using standard litho procedure, and masked using the Trenches mask. The SiO<sub>2</sub> was patterned using BOE, and the resist removed in acetone/IPA rinses. One wafer was cleaved into two 1/4 sections, and one 1/2 section, and the 2nd wafer left full. Standard etch settings were used to process the samples.

Etch data is completely dependant on the feature size, feature density, and the amount of Si in the etch chamber. This data is to be used as a guideline only; different samples with different amounts of exposed Si using different feature sizes will etch at different rates. It's recommended that the etch rates and any selectivity issues be determined using test pieces prior to etching samples, where possible.

Other users have used XeF<sub>2</sub> to release membranes using amorphous silicon as the sacrificial layer. A 500nm thick a-Si layer was etched ~180um from a 10um wide trench in 35 pulses. The etch rate is unlikely to be linear due to transport effects of the etch gas and SiF<sub>4</sub> etch byproduct.

Uniformity across the wafer is quite variable, most notable are the differences between the centre and the outer areas. This is likely due to localized consumption of the F. Also notable is the slight increase in depth of the area closest to the inlet (6.4um measurement).

