KOH and TMAH Etching of Bulk Silicon

Recipes, Tricks, What is Possible, and What is Impossible

K. Westra

February 11, 2010

1) General:
KOH and TMAH are anisotropic silicon etches, used to make V-grooves, membranes, and holes through wafers, as well as other devices. This is an 'old' technology for MEMS (30 years +), it is used a fair amount, but many advanced applications are still not possible, even after the 100's of papers published on the etch processes.

KOH and TMAH are close relatives. KOH is simply the hydroxide of potassium. TMAH is a organic hydroxide and stands for Tetramethyl ammonium hydroxide. KOH for etching comes in bottles of 45% by weight concentration and TMAH comes as 25% by weight concentration. Out of all the hydroxides, KOH etches the nicest.

2) Wafers
When etching into Silicon using KOH or TMAH, always use prime wafers. If you are doing a shallow etch, single sided polished is fine, but to go through a wafer or remove a large part of a wafer, double sided is needed to do the alignment.

The reason why prime wafers are needed is that the 'history' of the wafer is critical to the quality or the etch (or if it will etch at all). The cheaper wafers (coin rolled and test), are lower quality with often doped areas that can cause etch rate changes or the flats on the wafers are cut at the wrong angles and the devices can not be formed. Prime wafers have a known history and are high quality, so these issues are less of a problem.

3) (100) plane Etching and Masking Layers
Most often KOH and TMAH etches are used to etch the (100) plane, forming the membranes, V-grooves and other structures. The side walls of the etch are defined by the (111) planes. The angle between the sidewalls and the (100) plane is 54.7 degrees. Any MEMS textbook is a good resource for more details.

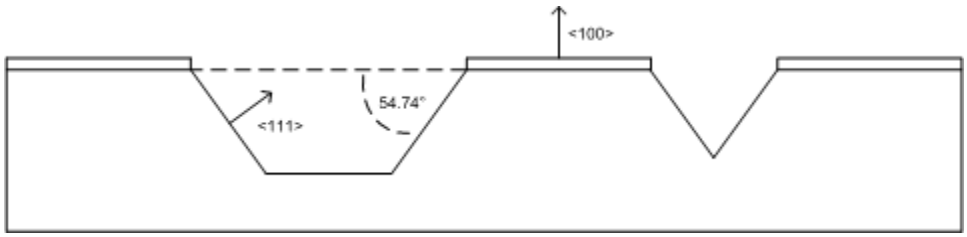

Figure 1. Typical side profile after anisotropic etch

The major flat on the wafer is aligned carefully (via the microscope) to the opening in the mask. This ensures the etched areas are bounded by the (111) planes. With

care you can align to ~0.2 degrees and the specification on the wafers is that the major flat is with in 0.5 degrees of the (111) planes.

Keep in mind that KOH and TMAH will etch any exposed silicon. A masking layer may need to be applied to the backside of the wafer or a carrier used that will protect the backside.

a) Shallow KOH etch:

- Etch solution is 32% KOH by weight
- Heat to 95 degrees C with stir bar slowly stirring
- Add wafer to be etched
- Etch rate ~1.0um/min
- Masking layers: SiO_2 (thermal) or SiN_x
- KOH etches SiO_2, mask will only last for <50um deep Si etch
- SiO_2 masking layer can be removed with BOE (buffered oxide etch)

b) Deep KOH etch

- SiN_x mask will survive etch a deeper etch (through wafer - 50um)
- SiN_x masking layer can be removed by dry etch (fast) or by a long soak in BOE (>8hrs)

c) TMAH etch (shallow or deep)

- Use 25% TMAH (no dilution)
- Heat to 95 degrees C
- Wafers must be BOE dipped for 30 seconds to remove native oxide in opened areas (TMAH will NOT etch SiO_2, even nanometers of native oxide)
- Etch rate: ~0.6um/min
- Mask: SiO_2 (Thermal)

4) Smoothness of (100) surface

The normal surface after a KOH etch often looks like an orange peel. A TMAH etched surface can not only have the orange peal surface, but can also have pyramids left. These are areas that did not etch due to either local masking by dirt, or SiO_2 that wasn't removed or that is found within the wafer.

To smoothen the (100) surface, there are a number of 'tricks' that can be used:

1. Add IPA to the solution. Ensure that a layer of IPA remains on top of the KOH or TMAH solution during the entire etch. The etch rate of KOH and TMAH will drop significantly.
2. Tilt the wafers to make it easier for the hydrogen bubbles to come off the surface (this is a cause of the roughness)
3. Add a surfactant. There are recent papers that gives the best surfactants for KOH and TMAH. The papers are in the journal "Sensors and Actuators A", as well as the latest work in this field

5) (111) to (100) ratio …. The Undercut

The ratio of (100)/(111) etch rates vary in the literature from 20:1 to 200:1. In my experience, 25:1 to 35:1 are realistic. This ratio describes the undercutting of the

masking layer as the (100) plane etches. The higher the ratio; less the undercut. Most applications would like no undercut, but that does not seem possible.

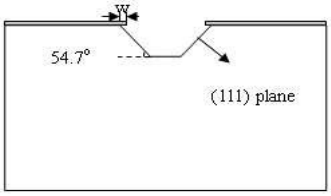

Figure 2: Undercut in anisotropic etching (W)

The reason for the large variation in the literature is not clear and not investigated. My personal opinion is that it is related to the accuracy to which the sidewalls of the mask layer are parallel to the (111) plane. The closer the edge is to parallel, the lower the rate. However, given the 0.5 degree unknown in the flat to (111) plane in the wafer and 0.1-0.2degrees in the alignment of the mask to the major flat, gives plenty of room for a significant non parallel mask edge to the (111) plane. Another reason could be a non straight mask edge, but rather a rough mask edge, due to poor lithography, which allows for greater undercut.

6) Etching structures that require higher order planes (points, flat areas, compensation structures)

Etching structures that use the higher order planes (i.e. features that are left above the (100) etched surface), this is an area of very little solid knowledge. Which plane that appears after the etch is not certain. The (411), (114), (311), (5,5,12) and many others have been identified in the literature.

It appears that the higher order planes that appear depend on the contaminates in the KOH and TMAH baths (HCO_3, Na, B, and others), mask placement, mask shape, age of bath, and others. The only advice I can give after etching 100's of wafers is that if you need compensation structures or sharp AFM tips, is to try it a few times and determine what works best to achieve desired results.