Tanner EDA

L-EDIT FOR PHYSICAL DESIGN

Product Benefits

- Support today's demanding IC designs with physical design tools that maximize efficiency.

- Speed up design cycles with built-in productivity tools.

- Control every aspect of the editing process.

- Work on laptops for anytime, anywhere use and access.

- Save time with a solution which is easy to set up, manage and use.

- Reduce CAD managers' support burden for your physical design tools.

- Integrate with third-party tools and legacy data through support for industry standard formats.

- Benefit from flexible licensing options.

Product Features

- Complete hierarchical physical layout including all-angle and curved polygons.

- Fast rendering.

- Import Cadence® Virtuoso® technology and display files.

- Object snapping (gravity).

- Interactive (real-time) DRC.

- Schematic Driven Layout (SDL) that uses netlist files in T-Spice™, HSPICE®, PSpice®, structural Verilog, or CDL formats.

- Easy to configure layout generators for the most common devices.

- Automatically create parameterized cells from layout.

- Node highlighting.

- LVS comparison.

- Standard cell place and route (SPR).

- Powerful UPI lets you create macros to automate common tasks.

- Multiple language support including English, Japanese, Simplified and Traditional Chinese, German, Italian, and Russian

Speeding Concept to Silicon

In today's analog design world, speed is more important than ever. To compete in a high-efficiency, high-productivity marketplace, you need a toolset that has proven its ability to accelerate the design cycles of commercially successful projects.

Tanner EDA's L-Edit™ meets your needs by combining the fastest rendering available with powerful features that exceed the needs of the most demanding user. This leading analog/mixed signal IC design tool for the PC platform enables you to get started with minimal training. You can draw and edit quickly, with fewer keystrokes and mouse clicks than other layout tools. Using powerful features such as interactive DRC, object snapping, and alignment, you can work more efficiently to save time and money.

L-Edit increases your productivity by enabling you to import Cadence® Virtuoso® technology and display files for quick setup. Save time by

using foundry-provided files directly, allowing you to avoid having to set up technology information manually. Once you've begun using L-Edit, the CAD support burden for your physical design tools will be reduced, enabling you to focus on other mission critical tasks.

Create layout with precision

L-Edit gives you greater precision by enabling you to perform complex Boolean and derived layer operations with polygons of arbitrary shape and curvature. Perform AND, OR, XOR, Subtract, Grow, and Shrink on groups of objects. You can display coordinate and distance values in any technology unit, and automatically add guard rings around any shape. Further increase your productivity by mapping multiple layout functions to a single keystroke.

- Perform complete hierarchical physical layout with all-angle and curved polygons on an unlimited number of layers.

- Use orthogonal, 45°, all-angle, and curved drawing modes.

- View your design with the fastest rendering on the market.

- Use a command line interface for run-time automation.

L-Edit schematic driven layout (SDL) provides capabilities that enable you to:

- Read in a netlist and automatically generate parameterized cells and instance them into your design.

- Display flylines allowing you to place your blocks to minimize routing congestion.

- Mark existing geometry as part of a specific net allowing selection and rip-up of geometry by net.

- Perform engineering change orders (ECO) and highlight differences in the netlists.

- Use netlist files in T-Spice™, HSPICE®, PSpice®, structural Verilog, or CDL formats.

L-Edit also supports parameterized cells called T-Cells™. With T-Cells, you can create versatile source cells that consist of user-defined input parameters and layout-generating code. T-Cells extend traditional geometry cells to include the flexibility and automation of L-Edit's user-programmable interface (UPI).

L-Comp™, a set of high-level composition functions, provides a simple toolkit for creating T-Cell code. Use L-Comp to efficiently create, place, and align cell instances in a design.

Navigate efficiently

L-Edit provides a built-in Design Navigator that enables you to:

- Efficiently traverse design hierarchy with top-down and bottom-up hierarchical view, non-instanced cells view, or view cells sorted by their modified date.

- Drag and drop cells into layout from library files, other design files, or the current design database.

- View layout details down to any level of the hierarchy.

- Lock and unlock cells to protect the design from any changes.

- Easily replace instances of one cell with another cell, at the current level or throughout the design.

- Maximize IP reuse or partition your design for multiple designers with L-Edit's multiple library support (XrefCells).

Gain complete control over editing

L-Edit gives you the flexibility and control you need to master the editing process. You can dramatically streamline the process by editing the properties of multiple objects simultaneously. With L-Edit you can instantly push down the hierarchy to any object, making it easy to edit edges, corners, and arcs. You can quickly stretch or shrink multiple edges to make room for more layout.

- Change the current drawing layer directly from the layout using the virtual layer palette.

- Perform unlimited undo and redo operations.

- Perform all-angle rotate, flip, merge, nibble, and slice operations.

- Speed drawing and editing by snapping the cursor to object vertices, edges, midpoints, center points, and instances.

- Perform one-click horizontal or vertical object alignment, equally space objects, or tile objects horizontally, vertically, or in a 2D array.

- Specify a reference point for editing operations such as object rotation, flip, move, or instance placement using the base point feature.

Work in a versatile environment

Save time and money with L-Edit's ease-of-use benefits:

- Delivers powerful features from an affordable, customizable, easy-to-manage tool.

- Offers a short learning curve.

- Enables you to import and export GDS, DXF, and CIF file formats.

- Provides multi-language menus (English, Japanese, Simplified and Traditional Chinese, German, Italian, and Russian).

- Customize and filter the Layer Palette to show only layers used in the file, current cell, or cell and its hierarchy allowing you to finish your layout faster.

- Enables you to easily cut and paste layout into your documentation flow.

Generate layout for parameterized devices

L-Edit's DevGen feature provides layout generators for most common devices. It is easy to configure for any process to help ensure DRC correct layout. Devices include Capacitor Generator, Inductor Generator, Resistor Generator, and MOSFET Generator. For specialized devices, use L-Edit's automatic layout to T-Cell generator to quickly complete your T-Cell library.

Create UPI macros

L-Edit's powerful user programmable interface (UPI) allows you to create macros that automate layout manipulations, geometric synthesis, batch verification, and advanced analysis. You can further increase your productivity by mapping multiple layout functions to a single keystroke. UPI macros are written in C/C++ language and can be executed with L-Edit's built-in interpreter or compiled as a DLL.

Speed layout with standard cell place and route

L-Edit standard cell place and route (SPR) performs place and route, padframe generation, and pad routing. To minimize total area, a built-in placement and routing optimizer automatically reduces net length and the number of vias. L-Edit SPR includes:

- Three-layer channel routing.

- Cell clustering options.

- Specification of critical nets.

- Global signal routing for clock nets.

- Back annotation with SDF.

- EDIF input.

Further streamline verification with Interactive DRC

L-Edit Interactive DRC displays violations in real time while you edit your layout, helping you create compact, error-free layouts the first time. Interactive DRC simultaneously checks for violations between objects in the same cell and down through the cell hierarchy.

Correct layout as you go

L-Edit Node Highlighting offers node highlighting for connectivity visualization so you can quickly find and fix LVS problems.

- Point to an object in the layout, regardless of hierarchy, and display all the geometry connected to it based on a set of connectivity rules.

- Highlight discrepancies between the schematic netlist and the extracted netlist in the layout.

- View multiple nodes in different colors.

- Track down shorts and opens.

- Improve design productivity significantly during LVS.

Verify complex designs with DRC

L-Edit DRC™ is a high performance, all-angle, hierarchical design rule checker. Setting up rules is configurable for any technology, with a graphical interface for easy setup. Hierarchical error output displays your errors at the level of the hierarchy where they occur, and the error navigator opens the cell and zooms automatically to the location of the error. Your productivity improves via speedy runtimes and quick location of errors.

L-Edit DRC features include:

- Support for an unlimited number of width, spacing, surround, enclose, extension, overlap, not exist, and density rules.

- High performance all-angle Boolean and Select layer generation.

- Flag offgrid vertices, self-intersecting polygons, all-angle edges, and polygons with more than a specific number of vertices.

- Full chip and local region DRC.

- Import of Calibre® DRC results for browsing in L-Edit.

- Seamless integration into the layout environment using the DRC Error Navigator.

Additional Productivity Features

· Cross-section viewer.

· Layout vs Layout comparison.

· Area calculator.

· PostScript mask export for high resolution transparency MEMS masks.

· Pad I/O cross reference for easy generation of bonding reports.

· High-resolution plotter support with the same rendering scheme used in L-Edit, including legends, rulers, and headers.

· Populate wafers with maximum number of die and label all dies on a wafer with WaferTools.

· CurveTools add chamfers and fillets quickly to your layout. It adds fillets of equal width to wires and processes multiple edges as a single edge when working with curved objects that have been converted to all-angle objects.

· LayerFill easily adds dummy fills to your layout to meet density requirements of deep submicron designs.

· MaskBias performs easy mask resizing on a layer by layer basis which is great for designs that are 65nm or below.

- See the DRC status (pass/fail/needed) of each cell.

Integrated Verification Error Navigator allows you to:

- Navigate instantly down the hierarchy to locate errors.

- View errors grouped by rule or by cell.

- See rule distance and actual violation distance.

- View errors in the top cell or in the cell where the error occurred.

- Mark or remove errors that have been fixed.

Extract SPICE netlists

L-Edit Extract™ generates a SPICE netlist from L-Edit layout for LVS comparison or for post-layout simulation with T-Spice. It extracts active and passive devices and user-definable subcircuits, with support for orthogonal, 45°, all-angle, and curved layout. To aid in verification against the schematic, L-Edit enables you to zoom or click in the layout to display a specific node or element. For increased accuracy, you can extract parasitic node capacitances, including fringing effects.

You can extract the most common device parameters, including:

- MOSFET width, length, source/drain area, and perimeter.

- Areas of diodes, BJTs, MESFETs, and JFETs.

- Capacitance and resistance.

- Subcircuit extraction for functional blocks with user parameters.

Compare layout to schematic

L-Edit layout versus schematic (LVS) accurately and efficiently compares two SPICE netlists to determine whether they contain equivalent circuit descriptions. LVS can use topological information, parametric values, and geometric values to compare netlists according to your specifications. The program quickly traces element and node mismatches back to their origins, pinpointing irresolvable nodes and devices using fragmented class reporting.

LVS offers a full range of pre-processing options to optimize netlists for comparison, including:

- Merging of parallel or series devices, where options can be set independently for different device types and for specific device models.

- Elimination of shorted and disconnected (open) devices.

- Elimination of parasitic resistors and capacitors that exceed user-supplied min/max thresholds.

- Removal of user-specified device models so that the nodes spanned by their terminals can be shorted or opened.

- Omission of user-selected device parameters from the compared netlists.

- Checking for soft-connections.

- Supporting asymmetrical MOSFETs with user-defined pin swapping.

- Matching device parameter values, which are crucial for analog design.

- Specifying pre- and post-iteration matches to speed the comparison process.

LVS reads netlist files in T-Spice, HSPICE, PSpice, or CDL formats, with support for all device types and key parameters. Input netlists do not need matching formats or hierarchy to be compared. LVS supports length and width parameters, with accompanying model definitions, in capacitor (C) and resistor (R) device statements.

Zip through LVS with cross-probing from SPICE and LVS results to layout or schematic and with enhanced navigation of SPICE files.

Benefit from flexible licensing

When you purchase a new design tool, licensing options can greatly affect your total cost of ownership. L-Edit is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, L-Edit will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, L-Edit does not have geographic restriction on its licenses, thus, lowering your total cost of ownership.

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