High Aspect Ratio DRIE on the STS ICP-RIE

Aspect Ratio Dependant Etching (ARDE) is the difference in the etch depth of features with varying areas of silicon. Areas with more open silicon etch faster compared to areas with lower amounts of open areas, such as in trenches and small width features. There are several possible explanations for this, such as ion flux loss at the bottom of a feature, and transport effects. The causes of ARDE have been discussed at length.¹ ² ³

Test wafers were prepared using standard cleaning (piranha, BOE) and lithography processes. A 1.3um SiO2 layer was grown and used as the Si etch mask. The SiO2 was patterned with HPR504 and etched in the STS RIE for 6 minutes. The HPR504 was removed used an acetone/IPA rinse, followed by ashing in the Branson etcher to remove residual resist. The test masks used contained varying amounts of exposed silicon, ranging from 2% to 90%, and contained trench and square features. Arrays of trenches consisted of 1um, 2um, 5um, 10um, 20um widths with different spacings between the 1um and 2um wide trenches. Data was collected using features located on the centre die.

The wafers were etched for 200 cycles using the Fast_Etch recipe on the STS ICP-RIE. After etching, the SiO2 mask was removed in BOE and the wafers were cleaved and imaged using the SEM. The measurement tool was used to measure etching depths and trench width openings. Below are the SEM images:

Figure 1: 1um wide trenches etched to a depth of 60.8um. AR = 36 due to the real trench width being 1.72um wide due to the change from prior processing.

The scallops along the sidewalls are quite large near the surface of the Si, and become significantly smaller as the etch depth increases, indicating a slowing etch rate throughout the etch, until etching is halted due to gas transport limitations. The “V” shaped trench bottoms are indicative of this phenomena.
Figure 2: “V” shaped trench bottoms due to gas transport limitations.

Figure 3: Notice the width of the opening; theoretical width is 1.0um, but through processing, has been decreased to 0.735um, and quickly increases just below the wafer surface to 1.724um before slowly decreasing as etch depth increases.
Figure 4: 5µm and 2µm wide trenches etched to depths of 115.6µm and 82.8µm respectively. AR = 23.1 for 5µm features and AR = 41.4 for 2µm features. This image is a good example of ARDE and microloading.

Figure 5: 20µm and 10µm wide trenches etched to depths of 179.9µm and 144.2µm respectively. AR = 9.0 for 20µm features and AR = 14.4 for 10µm features.
The amount of silicon exposed during etching will also affect the etch rate. The table below illustrates the combined effects of aspect ratio and exposed Si area and each effect on etch rate. Note – these etches were performed using the NanoFab’s standard silicon etch process, and will be different for each user. This data is to be used as a guideline only.

<table>
<thead>
<tr>
<th>% Exposed Si</th>
<th>2um</th>
<th>5um</th>
<th>10um</th>
<th>15um</th>
<th>20um</th>
</tr>
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<tr>
<td>2</td>
<td>0.89</td>
<td>1.06</td>
<td>1.20</td>
<td>1.29</td>
<td>1.35</td>
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<tr>
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<td>0.84</td>
<td>1.01</td>
<td>1.14</td>
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<tr>
<td>26</td>
<td>0.85</td>
<td>0.93</td>
<td>1.03</td>
<td>-</td>
<td>1.14</td>
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<tr>
<td>90</td>
<td>0.56</td>
<td>0.69</td>
<td>0.78</td>
<td>0.81</td>
<td>0.86</td>
</tr>
</tbody>
</table>

Table 1: Etch Rate of varying aspect ratios and exposed Si area

Using the standard Bosch etch recipe on the STS, current maximum aspect ratios of ~36:1 have been obtained. This is the maximum achievable aspect ratio do date, and further testing will need to be performed to improve this value. The STS does have the option to ramp parameters throughout a process, and is a good starting point for higher AR development. Suggested ramp rates could be: -0.1% reduction in pressure, 0.1% increase in Bias Power, and 0.05% increase in etch cycle time.
References:

1. Control of Aspect Ration Dependant Etching (ARDE), STS paper, 2003


3. Low frequency process for silicon on insulator deep reactive ion etching, Wasilik, Pisano, Berkeley Microlab.


5. Sensitivity, Loading Effects and ARDE Studies on the STS ICP-RIE, NanoFab document