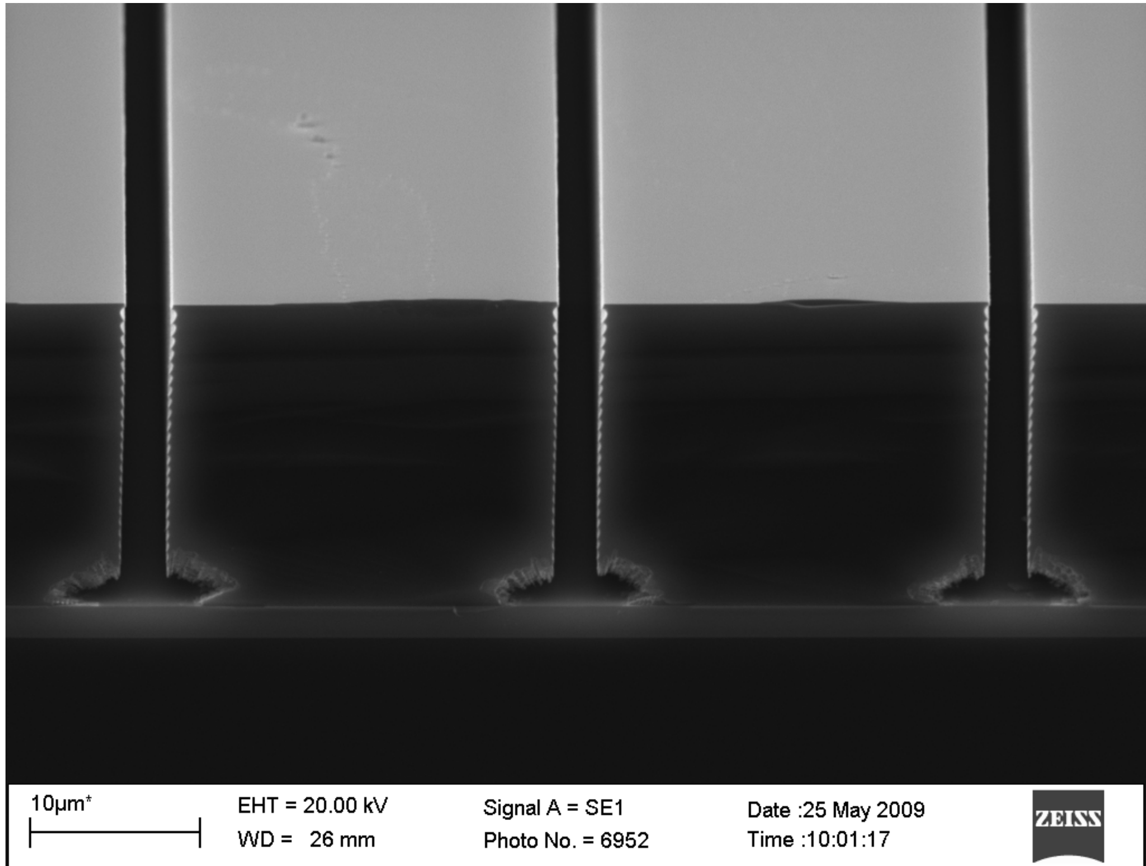
SOI Wafer Notch Reduction using the Low Frequency Pulsing Option on the STS ICP-RIE

At the University of Alberta's NanoFab



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The STS ICP-RIE is a dedicated silicon etcher, used to etch silicon to varying depths as required, ranging from tens of nanometers to hundreds of micrometers. Certain devices require the use of a buried dielectric layer, typically silicon dioxide (commonly referred to as silicon on insulator or SOI). The buried silicon dioxide acts as an etch stop due to standard etching processes preferentially etching silicon over silicon dioxide.

When SOI devices are etched using standard Bosch[1] processes on the STS, an undesired effect commonly called notching or footing occurs. This notching is due to one or more of the following issues: etch uniformity, aspect ratio dependant etching[2,3] (ARDE), and microloading. Refer to the document "*Advanced Bosch Processing on the Oxford Plasmalab ICPRIE*"[4] for further information on these issues and other NanoFab specific process controls.

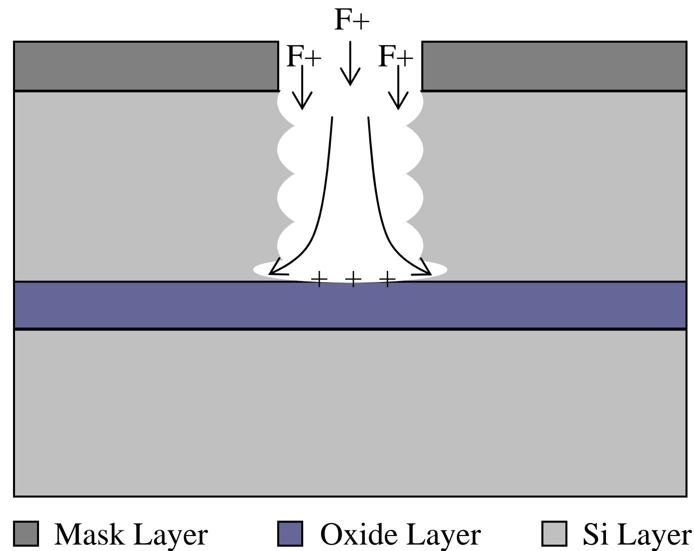


Figure 1: Charge build up on buried oxide layer; F+ ions repulsion.

Alternatively, surface notching may occur due to the formation of a native oxide layer on exposed silicon. The same charge build up and repulsion effects are occurring here, and may affect the etch depth that can be obtained due to mask lift off. Oxford Instruments has developed a technique called "Oxy-thermal Burst"[5] to eliminate this problem, but a quick BOE dip to remove the surface oxide just prior to processing will also eliminate this issue.

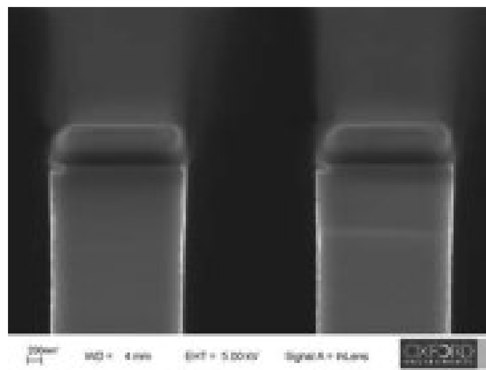


Figure 2: Notching at the surface of the wafer

One useful technique available on the STS ICP-RIE is the availability of a low frequency power supply, and the ability to choose between a pulsed or continuous mode. Standard Bosch etches typically use a 13.56MHz generator, while the low frequency option uses a frequency of 380MHz. By applying a lower frequency, the ions are allowed to escape the surface of the oxide, decreasing the charge build up, and reducing the notching.

The pulsed mode, when used in conjunction with the low frequency, enhances the reduction in charge build up. The pulsing will turn the platen power on and off at a desired time interval, and during the off step, the ions are allowed to escape, further reducing notching.

Results:

The images below display the difference between a high frequency etch and the low frequency pulsed etch. A range of trench widths were cleaved and imaged in the SEM. This set of SOI wafers had a device thickness of 20um, and buried oxide thickness of 1um, and a handle thickness of 400um.

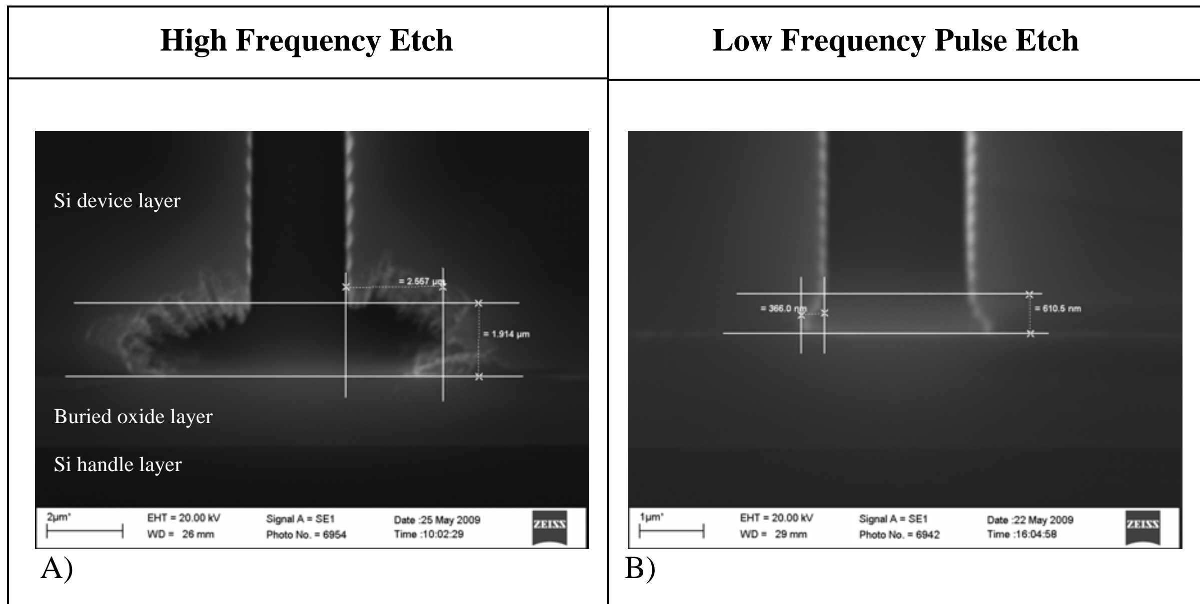


Figure 3: Si device layer etched to buried oxide, 2um wide trench opening.

A significant reduction in notching can be seen in figure 3. A) is using the standard high frequency etch, and B) is using the low frequency pulsed etch. Although the notching is reduced, there is still some optimization need to further reduce the effect.

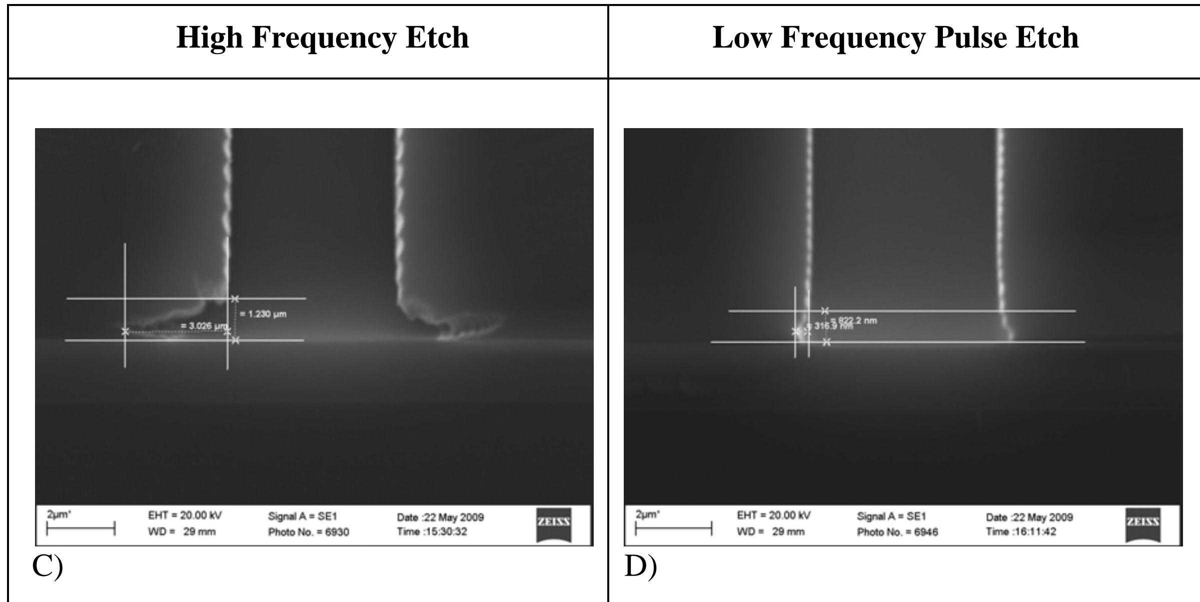


Figure 4: Si device layer etched to buried oxide, 5um wide trench opening.

A significant reduction in notching can be seen again in figure 4, this time on 5um wide trench openings. C) is using the standard high frequency etch, and D) is using the low frequency pulsed etch. Although the notching is again reduced, there is still some optimization need to further reduce the effect.

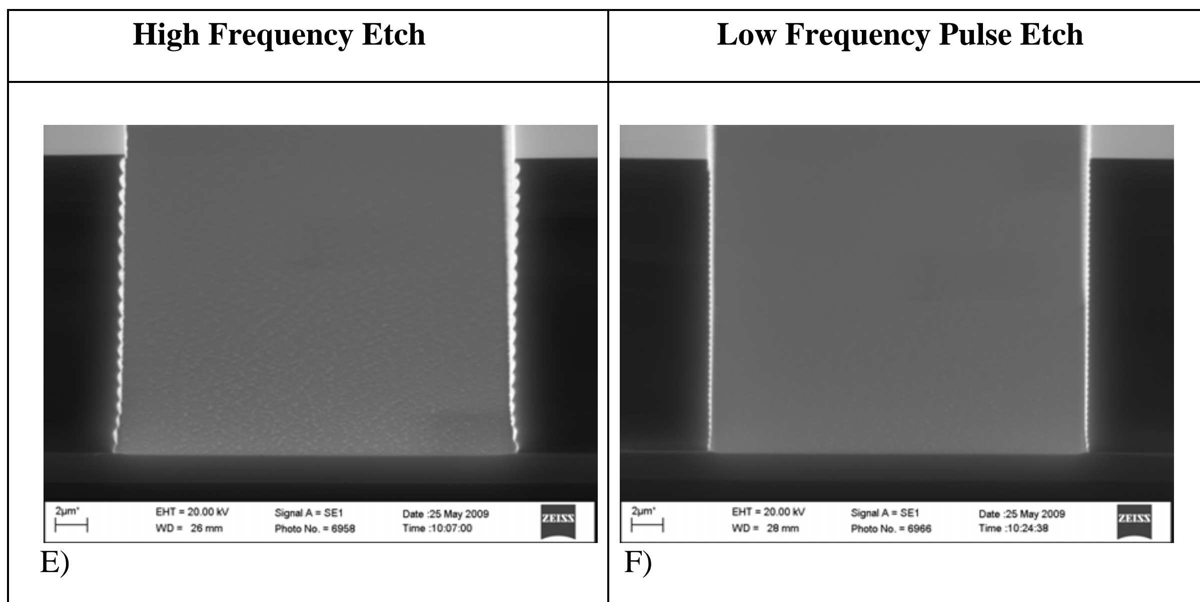


Figure 5: Si device layer etched to buried oxide, 25um wide trench opening.

As illustrated by the above images, the notching effect varies depending on the size of the trench opening. The 25um trench (E) indicates only a slight amount of notching compared to the 2um and 5um trench widths, where significant notching occurred. One

possible explanation[6] for the slight amount of notching in the 25um opening could be that the charge is dissipated over a larger area and not built up and confined to a relatively small area, where charging and repelling would be more likely to occur. Further optimization is necessary in this case to minimize the notching. Refer to appendix A for detailed recipe parameters.

The above recipe has been put into general use on the STS ICP-RIE and, as illustrated, will significantly reduce the notching effect when etching SOI wafers due to the combined effect of a lower frequency and pulsing the supply. Further optimization may be necessary, dependant on users design and the combined effects of ARDE, microloading and wafer uniformity. Users are encouraged to further develop or provide feedback with this or other processes on the STS.

References:

1. F. Larmer, A. Schlip, US Patent 5501893
2. Maximum achievable aspect ratio in deep reactive ion etching of silicon due to aspect ratio dependant transport and the microloading effect, Shannon et al, JVST B, (2005)
3. Control of ARDE, Surface Technology Systems USA
4. Advanced Bosch Processing on the Oxford Plasmalab ICPRIE, NanoFab
5. New Technique for Eliminating Mask Undercut in Cyrogenic Silicon Etching, D. Stephens, OIPT, Process News, spring 2009.
6. Low frequency process for silicon on insulator deep reactive ion etching, Wasilik, Pisano, Berkeley Microlab.

Appendix A

	Etch	**Passivate**
Step Time (s)	7.0	4.0
Overrun (s)	0.5	0.5
Power		
ICP (W) (@13.56MHz)	1500	1500
Platen (W) (@ 380KHz)	30	0
Range (W)	0-300	-
Pulse (ms)	5	-
Period (ms)	20	-
Gas Flows		
SF6 (sccm)	200	-
O2 (sccm)	20	-
C4F8 (sccm)	-	100
Pressure		
APC (%)	80	80
Platen Temperature (^{o}C)	10	10
HBC (T)	10	10

Table 1: SOI Pulse Etch recipe parameters

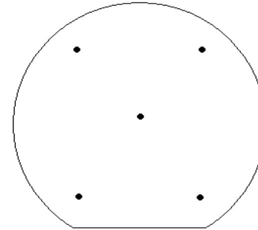
Low frequency pulsing options on the platen. The platen frequency can be set to either 13.56MHZ or 380KHz in the software, with parameters ranging from 0-300W. The Range option can set to either 0-30W or 0-300W, and is dependant on the platen power setpoint. The range should be set to 0-30W if the power is set to a value of 10W or less, and 0-300W if the power is set to >10W.

The pulse and period, as well as a pulse delay (which was not used in this round of testing) are changed on the control module located in the Subfab. To change these settings, first ensure the switch for the platen LF pulse mode is selected. Parameters are adjusted using dial settings on the control module. The period has a range of 100ns to 10s, the pulse width a range of 50ns to 5s, and a pulse delay range of 50ns to 5s. There are also various functions/modes available in addition to the pulse mode, including square, double pulse, and delayed pulse which were not used in this test.

Standard silicon wafers were used originally as test wafers to determine etch information. The wafers were etched using the recipe outlined in Table 1, and the following etch information was obtained:

Selectivity (Si:504)	33:1
Uniformity (%)	9.5%
Average Etch Rate (um/min)	2.3
Average Etch Rate (um/cycle)	0.43

Table 2: Etch results



The results in Table 2 are an average of five points measured across the wafer. HPR504 was used as the masking layer, and was created using standard cleaning and lithography techniques found in the NanoFab. A chamber condition was performed prior to etching, which involves running 25 cycles of a Bosch etch, labeled Conditn in the STS software.