

# Processing on the Oxford Estrelas

Sept 18, 2015



The Oxford PlasmaPro 100 Estrelas is the latest R&D deep silicon etch (DRIE) system offered from Oxford Instruments. The system is designed specifically for silicon etch processes, in both the nano and micro scales, and is capable of both Bosch and Cryo etching. The system was installed and qualified in 2015, and is currently available to users who require silicon etch processing. The system is configured for both 100mm and 150mm hardware configuration on a rotating schedule. Refer to the schedule for current and upcoming configurations.

To increase the likelihood of success when using the Estrelas, users should educate themselves prior to beginning a process. Below is a snippet of items to consider during when designing a process, as well as examples of some of the standard processes available on the Estrelas.

### Considerations:

**Selectivity and mask compatibility** – The masking material must be able to withstand the duration of the etch, as well as the etching conditions (ie. cryogenic temperatures).

**Uniformity** – The etching rate will vary depending on the feature location on the wafer, as well as feature sizes. Generally speaking, the etch rate is higher the closer to the edge of the wafer. Wafer and device layer thicknesses will also vary slightly, and must be considered when etching. Some sort of over etch is typically required to achieve the desired etch depth. When designing a mask, always minimize the amount of exposed area to improve uniformity.

Etch Rate – Again varies with features size (smaller features etch slower), as well as total exposed areas (larger exposed areas etch slower than masks with smaller exposed areas). Again, when designing a mask, always minimize the amount of exposed area to improve etching rates.



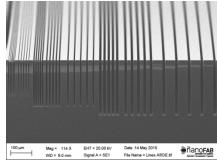
**Mounting** – mounting smaller pieces is a requirement due to the system being in either 100mm or 150mm mode. There are a variety of mounting materials available, ranging from tapes, greases and photoresists. Always ensure the mounting material is vacuum compatible, and can withstand an etch process. A lot of heat is generated over the course of an etch, and for this reason, thermally conductive materials are recommended (Crystalbond, Dow340, vacuum grease/oil). For cleaner, but less thermally conductive processes, double sided release tape, kapton tape, or photoresist can be used.

Potential Issues and considerations: ARDE, grass/micromasking, SOI tuning and LF processing

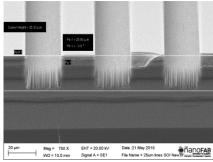
**ARDE** (aspect ratio dependent etching), is a known issue in the Si etch process. Generally speaking, smaller features will etch slower and will eventually stop etching altogether as the etch depth increases. This is due to a combination of etch gas unable to diffuse to the base of a feature, and etch by-products unable to escape.

**Grass/Micromasking** – Generally caused by an improperly tuned etch recipe, re-sputtered masking materials (notably metals, which are not recommended), poor lithography or poorly performed steps done prior to DRIE work. Grass is most common on open areas, and it is recommended that the amount of open area be minimized when designing a mask to improve the chance of success of the DRIE step.

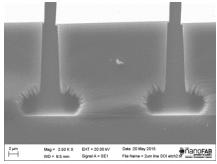
**SOI Device layer etching** – When etching to a buried oxide layer, a low frequency (990Hz) generator is available for etching. The LF generator will reduce the amount of notching when the SiO2 layer is reached. Shallower etches (<20um) are able to use the LF for the duration of the etch, but if etching >20um, it is recommended to use the HF generator for the bulk of the etch, then to switch to the LF when reaching the SiO2 layer. The LF generally processes at reduced selectivities and etching rates.



Example of ARDE



Grass formation on open areas

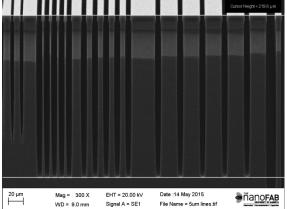


SOI wafer with overetch and subsequent notching – use LF to minimize

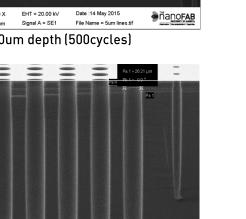


Etch Recipe - High Rate - Single Stage - Ideal for open area features. Smaller features with <50um openings tend to have a closing profile at depths >300um. Use 2 or 3 stage for smaller features and large depths.

500cycles Bosch High Rate, 100mm Si wafer with AZP4620 mask. Low exposed area, <50um features



5um lines, 220um depth (500cycles)

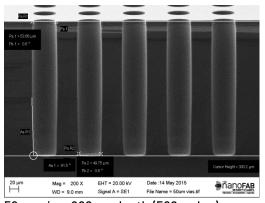


File Name = 25um vias.tif

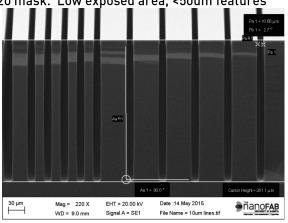
nanofab

25um vias, 246um depth (500cycles)

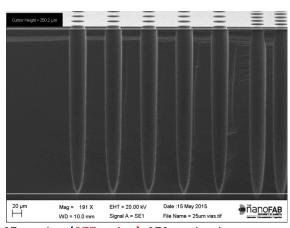
Signal A = SE1



50um vias, 300um depth (500cycles)



10um lines, 261um depth (500cycles)



25um vias, (875cycles), 350um depth

Etch Rate: 0.6um/cycle, 10.7um/min

Selectivity: 115:1 (Si:AZP4620)

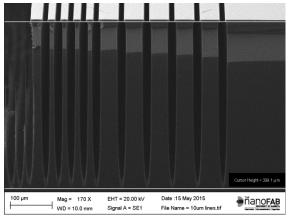
Uniformity: <5%

-Data measured using 50um via.

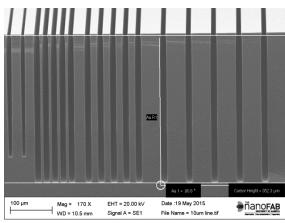


Etch Recipe - High Rate, 2 and 3 stage - Recommended for processes requiring deeper (>300um) etches of smaller open area features to maintain vertical sidewalls.

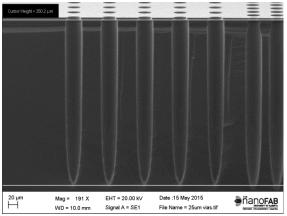
## 2 Stage (400 + 400 cycles) process results:



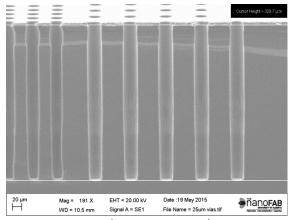
Single stage high rate (875 cycles), 10um lines etched to 399um (for comparison)



2 stage high rate (400 + 400cycles), 10um lines, etched to 352um



Single stage high rate (875cycles), 25um vias etched to 399um (for comparison)



2 stage high rate (400 + 400cycles), 25um vias etched to 330um

Etch Rate: 0.52um/cycle, 11.2/min

Selectivity: 80:1 (Si:AZP4620)

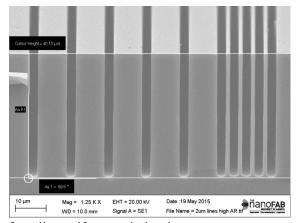
Uniformity: <5%.

-Data measured using 50um via.

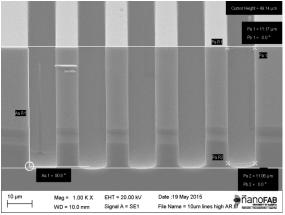


Etch Recipe - High Aspect Ratio Etch - Recommended for processes with small feature sizes (<10um) that require deeper etches. Open areas will likely form grass.

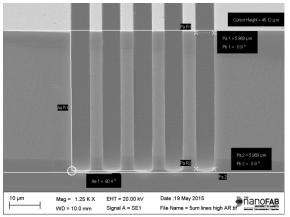
170 cycles High Aspect Ratio, SiO2 etch mask



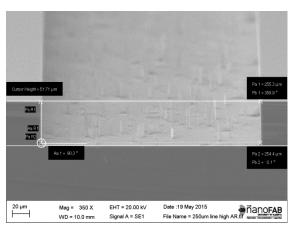
2um lines, 40um etch depth



10um lines, 49um etch depth



5um lines, 46um etch depth



250um line, 52um etch depth, grass formation

Etch Rate: 0.24um/cycle, 7.3um/min

Selectivity: 300:1 (Si: SiO2)

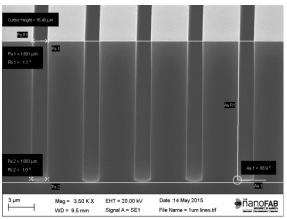
Uniformity: <5%.

-Data measured using 2um lines.

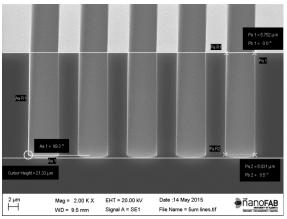


Etch Recipe - Smooth Sidewall Process - Ideal for processes requiring smoother sidewalls (optical work, polymer master fabrication). The rate etching rate is reduced compared to the previous etches, but with <25nm scallop.

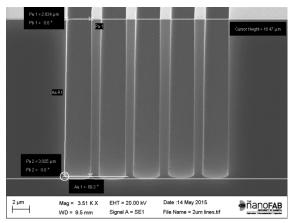
200 cycles using Smooth sidewall process, SiO2 masking layer.



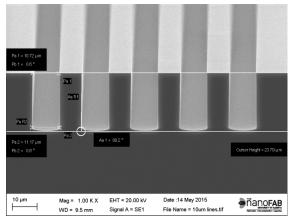
1um lines, 16.4um etch depth



5um lines, 21.3um etch depth



2um lines, 18.5um etch depth



10um lines, 23.8um etch depth

Etch Rate: 0.1um/cycle, 4.7um/min

Selectivity: 33:1 (Si: HPR504)

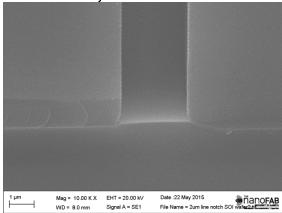
Uniformity: <5%.

-Data measured using 5um lines.

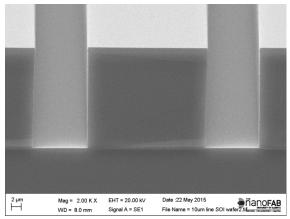


Etch Recipe - SOI Process - Uses the LF (990KHz on platen) to minimize the notching effect when etching to a buried SiO2 layer. Over-etching is typically required to compensate for ARDE and uniformity issues. The etch is quite selective to SiO2, and will slow (not stop completely) on the BOX layer. If etching >20um, it is recommended to use a recipe that uses the HF platen supple for the bulk of the etch, and switch to a LF recipe to reach the BOX layer to improve etching rates and selectivity.

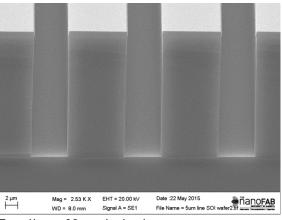
SOI Etch - 120 cycles



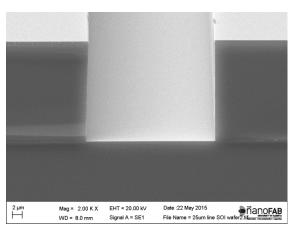
2um line, 20um device layer



10um line, 20um device layer



5um lines, 20um device layer



25um line, 20um device layer

Etch Rate: 0.16um/cycle, ~7.1um/min

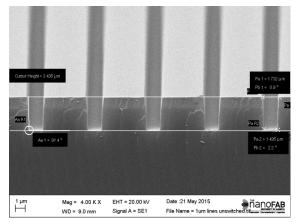
Selectivity: 53:1 (Si: HPR5040)

Uniformity: <5%.

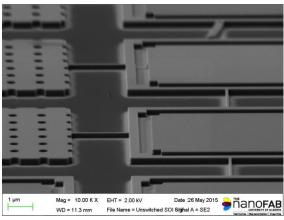


Etch Recipe - Unswitched Process - A continuous etching using both etch and passivation gases to achieve smooth sidewalls. Ideal for shallow etch processes. Etching rates are slow (<1um/min), and selectivity is poor (~10:1 to standard resists). The profile can be tuned by adjusting the ratio of gases (SF6:C4F8)

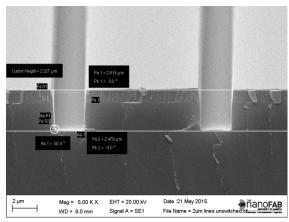
## Process time of 4min, HPR504 etch mask



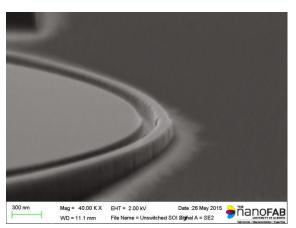
1um lines, 2.4um etch depth



SOI - 220nm device layer, 20s etch time



2um lines, 2.3um etch depth



SOI - 220nm device layer, 20s etch

Etch Rate : 0.58um/min

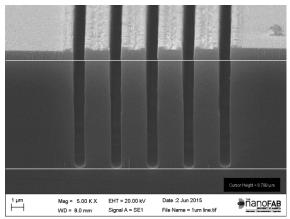
Selectivity: 11:1 (Si: HPR504)

Uniformity: <5%.

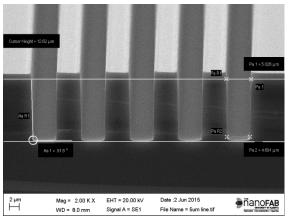


Etch Recipe - Cryogenic Etch - Another mixed gas process, similar to the unswitched process. Cryo processes require a compatible mask, as standard resists do not withstand the cold chuck temperatures (-100C), and crack or delaminate. Thinner resist masks (HSQ, ZEP etch), or hard masks (SiO2, Al2O3) are recommended.

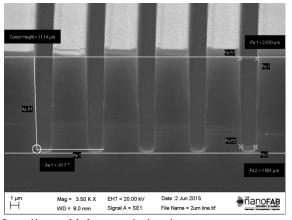
## 3min Etch process, SiO2 masking layer



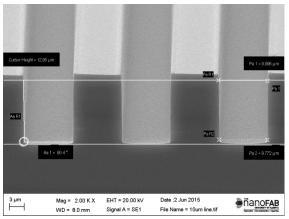
1um lines, 8.8um etch depth



5um lines, 12.6um etch depth



2um lines, 11.1um etch depth



10um lines, 13um etch depth

Etch Rate: 4.2um/min Selectivity: 62:1 (Si: SiO2)

Uniformity: <5%.

-Data measured using 5um lines.